UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,878	08/20/2001	Ichiro Kono	XA-9542	4052

7590 01/23/2003

Miles & Stockbridge P.C.
Suite 500
1751 Pinnacle Drive
McLean, VA 22102-3833

EXAMINER
CHANG, DANIEL D

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,878	KONO, ICHIRO	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *25 November 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on November 25, 2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Giles et al. (US 5,015,875).

Regarding claim 1, Giles et al. discloses, in fig. 2, a storage circuit (12) comprising:

a first logic gate (20, 22) for receiving a first signal (SD1) and a second signal (D), and for selectively outputting either the first signal or the second signal in accordance with a control signal (SE);

a first storage element (34/36) for receiving a clock signal (CK), for storing an output signal (62) of the first logic gate in response to the clock signal, and for outputting the stored signal as a third signal (signal at node 74) in response to the clock signal; and

a second logic gate (52) for receiving an output signal (78) of the first storage element, said second logic gate fixing (pass or block by pass gate 52) an output signal (signal at node 80) thereof, regardless of the received third signal, in response to the control signal (SE);

wherein the storage circuit, having a first output (Q) and a second output (SD0), outputs the third signal (signal at node 74) through the first output (Q), and the output signal of the second logic gate (52) through the second output (SD0).

Regarding claim 17, Giles et al. discloses, in fig. 2, a storage circuit (12) having first (Q) and second outputs (SD0) comprising:

a first logic gate (20, 22) for receiving a first signal (SD1) and a second signal (D), and for selectively outputting either the first signal or the second signal in accordance with a control signal (SE);

a first storage element (34/36), having a master latch (34, 36) and a slave latch (38, 40), wherein the master latch inputs an output signal of the first logic gate (62) and latches the output signal of the first logic gate in response to the clock signal, and the slave latch inputs an output signal (74) of the master latch and passes the output signal of the master latch to the first output of the storage circuit in response to an inverted clock signal (30);

a second logic gate (52) for receiving an output signal (78) of the master latch (via 38, 32), and for outputting the output signal of the master latch (via slave 38, 40) to the second output of the storage circuit in response to the control signal (SE).

Regarding claim 18, Giles et al. discloses, in fig. 2, a storage circuit (12) comprising:

a first logic gate (20, 22) for receiving a first signal (SD1) and a second signal (D), and for selectively outputting either the first signal or the second signal in accordance with a first control signal (64);

a first storage element (34/36) for receiving a clock signal (CK), for storing an output signal (62) of the first logic gate in response to the clock signal, and for outputting the stored signal as a third signal (signal at node 74) in response to the clock signal; and

a second logic gate (52) for receiving the third signal (via 38 and 32) from the first storage element, said second logic gate fixing (pass or block by pass gate 52) an output signal (signal at node 80) thereof, regardless of the received third signal, in response to a second control signal (60);

wherein the storage circuit, having a first output (Q) and a second output (SD0), outputs the third signal (signal at node 74) through the first output (Q), and the output signal of the second logic gate (52) through the second output (SD0).

Regarding claim 19, Giles et al. discloses, in fig. 2, that wherein the second control signal (60) is fixed to a low level (when SE=LOW) earlier than the first control signal (see inverter 28) at a time of a transition from a scan-in operation (SD1) to a logic test operation (D).

Allowable Subject Matter

Claim 20 is allowable over the prior art.

Response to Arguments

Applicant's arguments with respect to claims 1, 17-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ebzery (US 5,444,404) discloses a scan flip-flop with power saving feature.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Daniel D. Chang
Primary Examiner
Art Unit 2819

DC
January 21, 2003

DANIEL CHANG
PRIMARY EXAMINER